The Gap between Processor and Memory Speed

Computer Architecture

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Summary Report

The execution of the PC has been held by different components, among which one is the dissimilarity among the PC processor and the memory speeds. The usage of a Memory Hierarchical System, which exploits region and cost/execution of memory advances is one of the answers to limit this divergency. Additionally, the normal data transmission and the normal inertness are the real parameter that characterizes the attributes execution of the processor-memory. Infinite bandwidth and zero latency is the condition in which the greatest execution is accomplished and which is the base establishment for execution rate for the computational framework. In any case, the complexities between these two make it hard to decide if the memory-processor disparity is because of the absence of enough data transmission or crude memory inactivity. Cache memory has been presented between the microchip and the memory to cross over any barrier as it serves to increments in clock frequencies, pipelining, super-pipelining, superscalar - set expanding weight on the memory chain of command. As developing processor-memory performance gap is currently the primary obstruction, to enhanced PC framework execution planners have been applying cache advancement procedures that are Miss Rate Reduction Techniques, Miss Penalty Reduction and Hit Time Reduction. Ideas to put the memory and processor into a solitary chip have been proposed to determine this issue. New rising methods like intelligent memory could be the appropriate response that could take care of the key issues of the processor-memory execution gap by taking the benefit of the current advance in the transmission capacity DRAMs field and by joining a portion of the memory hierarchy of command streamlining systems. Additionally, applying memory pecking order techniques, change of bus controllers and the advancement of more quick-witted recollections could be a portion of the approaches to limit this dissimilarity and enhance the speed and execution of both the processor and memory.

References:

Carlos C. (January 2002). The gap between processor and memory speeds. Retrieved from: <https://www.researchgate.net/publication/228675147_The_gap_between_processor_and_memory_speeds>

Maniac G. (January 2005). Speed/performance gap between processor speed and memory/FSB speed. Retrieved from: <http://answers.google.com/answers/threadview?id=454373>

Bruce J. (2003). A case for studying DRAM issues at the system level. Retrieved from: <http://terpconnect.umd.edu/~blj/papers/micro23-4.pdf>

Fritz K. (March, 2016). CPU bandwidth – the worrisome 2020 trend. Retrieved from: <https://blog.westerndigital.com/cpu-bandwidth-the-worrisome-2020-trend/>

Maurice W. (June 2001). The memory gap and the future of high performance memories. Retrieved from: <http://www.cl.cam.ac.uk/research/dtg/www/publications/public/files/tr.2001.4.pdf>